Amendments to the Specification:

Please replace the paragraph beginning on page 35, line 17, with the following rewritten paragraph:

The interpolation/profile processing circuit 220 is provided with a G interpolation circuit 221, a band pass filter (BPF) 222, a clip circuit 223, a gain circuit 224, a low pass filter (LPF) 225, a color difference signal generation circuit 226, an interpolation/low pass filter (LPF) circuit 228, a matrix circuit 229, and adder 230 and a median circuit 232. The interpolation/profile processing circuit 220 performs format processing for JPEG data compression for individual data blocks corresponding to 20X20 pixel areas in the image data having undergone white balance fine adjustment to generate Y signals corresponding to ~~16X8~~ 8X8 pixel areas and Cb signals and Cr signals each corresponding to 8X8 pixel areas. A brightness signal Y contains a brightness signal Y1 indicating the low frequency component of the G signal and a profile extraction signal Y2 corresponding to the high frequency component of the G signal, as will be explained later.

Please replace the paragraph beginning on page 45, line 14, with the following rewritten paragraph:

The JPEG compression circuit 33 repeats the process in which as single unit of YCrCb signals formatted to correspond to the 8X8 pixels to facilitate the JPEG compression method based upon the Y signals corresponding to ~~16X8~~ 8X8 pixels generated by the adder circuit 230 and the Cr signals and the Cb signals corresponding to the 8X8 pixels generated by the median circuit 232 is extracted from input data corresponding to each 20X20 pixel area block input to the block processing circuit 20 and the extracted data are compressed through the procedure in the known art, until the entire image is compressed. The compressed image data are stored in the PC card 34 via the CPU 21.